

MEHDI BOUAMA

M2 SETI - Embedded Systems / FPGA / Digital Design

Orsay, France | +33 6 69 48 54 19 | mehdi.bouama.pro@gmail.com
linkedin.com/in/mehdi-bouama | github.com/mahdidou711

Profile

M2 SETI student at Université Paris-Saclay, specializing in Architecture. Experience spans FPGA/VHDL digital design and RTL verification, embedded C/C++ and Linux/Raspberry Pi integration, plus autonomous robotics and sensor/actuator interfaces. Seeking a 4- to 6-month final-year internship from March 18, 2027 in embedded systems, FPGA/SoC, digital design or hardware-software integration.

Technical Skills

FPGA / RTL Design: VHDL, FSMs, datapath design, processor architecture, digital arithmetic, Quartus, Vivado (mini-project).

Verification: VHDL testbenches, exhaustive verification, independent reference-model checking, GitHub Actions CI.

Embedded Systems & Software: C, C++, Python, Linux/Raspberry Pi, ESP32, STM32 (academic project), I2C, UART, PWM.

Tools: Git, CMake, Make.

Technical Projects

8-bit Multicycle Processor - RTL Verification & DE1 Port Preparation 2026

[GitHub repository](#)

- Extended an existing university RTL design (original FSM, ALU and datapath from coursework): built the verification environment, fixed the program-counter boundary behavior and prepared the DE1 port (wrapper, Quartus project, pin assignments).
- Verification: 1,573,888 exhaustive vectors on the ALU and its sub-units (0 errors, independent reference model), distinct from separate cycle-exact processor checks and GitHub Actions CI.

Sequential VHDL Cores - 16-bit Integer Square Root and Sequential Search 2026

[GitHub sqrt16](#) | [GitHub search/mult](#)

- Unsigned sqrt16 core: 8 iterations, `floor(sqrt(X))` result after **9 clock periods**; exhaustively verified all 65,536 inputs in RTL simulation against an independent reference model.
- Developed `searchx` core (historical DE1 test predates current input-capture fix; current version not board-tested); exhaustively verified in RTL simulation an 8x8 shift-add multiplier originally written by a fellow student (all 65,536 combinations).

CoVAPSy - 1/10-scale Autonomous Vehicle Jan. 2026 - May 2026

[GitHub repository](#)

- Raspberry Pi 4, RPLidar A2M12 (UART), SRF10 sonar (I2C), ESC/servo PWM; reactive Python control loop with a configured **50 Hz** rate.
- Navigation and control, LiDAR watchdog, stuck-recovery logic and CSV telemetry.

Other technical projects: STM32/ESP32 vehicles with custom PCBs; C/OpenMP/SIMD; RPN calculator in C99/CMake; C++ OOP / data structures.

Experience

Private Tutor - Self-Employed Sep. 2024 - Present

Mathematics, physics, electronics and programming; individualized tutoring from secondary school to post-secondary level, with exercises adapted to each student's needs.

Electrical Engineering Job-Shadowing Internship - EPTV, Algiers Jun. 2023

Two-week observation placement.

Education

Université Paris-Saclay - Master 2 SETI 2026 - 2027

Embedded Systems and Information Processing - Specialization: Architecture

Université Paris-Saclay - Master 1 E3A 2025 - 2026

Autonomous Systems, Embedded Intelligence and Information Processing

Université Paris-Saclay - Bachelor Year 3 (L3) E3A 2024 - 2025

Electronics, Electrical Energy and Automation Engineering

Bachelor's Degree - Electronics - USTHB, Algiers 2021 - 2024

Languages & Certifications

Arabic: Native | **French:** C2 - TCF | **English:** C1 - Linguaskill